WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor layer of a first conductive type formed in an active region;

a first gate electrode formed on the semiconductor layer via a gate insulating film in a predetermined pattern;

a first insulating mask formed on at least a part of the first gate electrode and a part of the semiconductor layer; and

a pair of first diffusion regions of a second conductive type formed in the active region not covered with the first insulating mask and first gate electrode, said pair of first diffusion regions being positioned adjacent to the first gate electrode and being used as a source and drain.

2. The semiconductor device according to claim 1, wherein said first gate electrode comprises an end portion arranged in the active region, and said first insulating mask is formed on said end portion of the first gate electrode and the semiconductor layer to cross the active region along a gate length direction of the first gate electrode.

3. The semiconductor device according to claim 2, further comprising a second diffusion region of the first conductive type positioned adjacent to the first insulating mask and formed at an opposite side of the

first diffusion region, said second diffusion region containing a higher impurity concentration than the semiconductor layer.

4. The semiconductor device according to claim 3, wherein said first gate electrode is arranged in a first direction and comprises a first portion and a second portion, said first portion is positioned under the first insulating mask, and a distance between an end of the first portion and an end of the semiconductor layer in a second direction vertical to the first direction is shorter than a distance between an end of the second portion and an end of the first diffusion region in the second direction.

5. The semiconductor device according to claim 3, wherein a second gate electrode, a second insulating mask and a third diffusion region are symmetrically formed to the first gate electrode, the first insulating mask and the first diffusion region, with respect to an axis of the second diffusion region; and

said first gate electrode is connected to said second gate electrode, and said first diffusion region is connected to said third diffusion region.

6. The semiconductor device according to claim 3, wherein said first diffusion region and said second diffusion region are separated at a predetermined interval, and said predetermined

interval is a width of the first insulating mask.

7. The semiconductor device according to claim 1, wherein said first gate electrode is formed across the active region, and said first insulating mask is extended from on the semiconductor layer of one of the pair of the first diffusion regions to on a part of the first gate electrode.

8. The semiconductor device according to claim 7, further comprising a second diffusion region of the first conductive type formed in the active region around the first insulating mask and positioned adjacent to one of the pair of the first diffusion regions, said second diffusion region containing a higher impurity concentration than the semiconductor layer.

9. The semiconductor device according to claim 8, wherein said first insulating mask is formed on an end portion of the active region.

10. The semiconductor device according to claim 8, wherein said first insulating mask is formed at a center of the active region.

11. The semiconductor device according to claim 8, further comprising a silicide film formed on a boundary surface between one of the pair of the first diffusion regions and the second diffusion region.

12. The semiconductor device according to claim 8, further comprising a contact formed on a boundary

surface between one of the pair of the first diffusion regions and the second diffusion region.

13. The semiconductor device according to claim 8, wherein said one of the pair of the first diffusion regions and the second diffusion region comprise a same potential.

14. The semiconductor device according to claim 7, further comprising a lattice defect region formed in a proximity of a boundary between the semiconductor layer under the first insulating mask and the one of the pair of the first diffusion regions.

15. The semiconductor device according to claim 14, further comprising a fourth diffusion region of the second conductive type formed on a surface of the active region under the first insulating mask, said fourth diffusion region containing a lower impurity concentration than the first diffusion region.

16. The semiconductor device according to claim 15, wherein said lattice defect region is also formed in the proximity of a boundary between the semiconductor layer and the fourth diffusion region.

17. The semiconductor device according to claim 1, wherein said first gate electrode formed on the semiconductor layer in substantially linear.

18. The semiconductor device according to claim 1, further comprising a spacer formed on a sidewall of the first gate electrode, said spacer being formed of

a same material as the first insulating mask.

19. The semiconductor device according to claim 1, further comprising an insulating film formed under the semiconductor layer.

20. A method of manufacturing a semiconductor device comprising:

forming an active region;

forming a semiconductor layer of a first conductive type in the active region;

forming a first gate electrode on the semiconductor layer via a gate insulating film in a predetermined pattern;

forming a first insulating mask on at least a part of the first gate electrode and a part of the semiconductor layer; and

forming a pair of first diffusion regions of a second conductive type using as a source and drain in the active region adjacent to the first gate electrode by using the first insulating mask.

21. The method of manufacturing a semiconductor device according to claim 20, wherein said first gate electrode comprises an end portion arranged in the active region, and said first insulating mask is formed on the end portion of the first gate electrode and the semiconductor layer to across the active region in a gate length direction of the first gate electrode.

22. The method of manufacturing a semiconductor

device according to claim 21, further comprising forming a second diffusion region of the first conductive type in the active region opposite to the first diffusion region by using the first insulating mask, said second diffusion region being positioned adjacent to the first insulating mask and containing a higher impurity concentration than the semiconductor layer.

23. The method of manufacturing a semiconductor device according to claim 22, wherein said first gate electrode is arranged in a first direction and comprises a first portion and a second portion, said first portion is positioned under the first insulating mask, and a distance between an end of the first portion and an end of the semiconductor layer in a second direction vertical to the first direction is shorter than a distance between an end of the second portion and an end of the first diffusion region in the second direction.

24. The method of manufacturing a semiconductor device according to claim 22, wherein a second gate electrode, a second insulating mask and a third diffusion region are symmetrically formed to the first gate electrode, the first insulating mask and the first diffusion region, with respect to an axis of the second diffusion region; and

said first gate electrode is connected to said

second gate electrode, and said first diffusion region is connected to said third diffusion region.

25. The method of manufacturing a semiconductor device according to claim 20, wherein said first gate electrode is formed across the active region, and said first insulating mask is extended from on the semiconductor layer of one of the pair of the first diffusion regions to on a part of the first gate electrode.

26. The method of manufacturing a semiconductor device according to claim 25, further comprising forming a second diffusion region of the first conductive type in the active region around the first insulating mask, said second diffusion region being positioned adjacent to one of the pair of the first diffusion regions and containing a higher impurity concentration than the semiconductor layer.

27. The method of manufacturing a semiconductor device according to claim 25, further comprising forming a lattice defect region in a proximity of a boundary between the semiconductor layer under the first insulating mask and one of said pair of the first diffusion regions.

28. The method of manufacturing a semiconductor device according to claim 20, further comprising forming a spacer on a sidewall of the first gate electrode simultaneously with the first insulating

mask.

29. The method of manufacturing a semiconductor device according to claim 20, wherein said semiconductor layer is formed on an insulating film.